GRANT



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Orchestration and Reconfiguration Control Architecture

D5.2: First toolset for reconfigurability/reprogrammability of SDR devices.

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Abstract	This deliverable provides an overview of the first toolset for reconfigurability and reprogrammability for SDR devices. Some of these toolsets are already made available publicly or through dedicated licenses. The supporting documentation is made available in the public ORCA portal.
Keywords	Software tools, SDR, live programming

ORCA SDR software toolsets developed in Y2 are made available via the ORCA portal webpage https://www.orca-project.eu/resources/software-components/, as shown in Figure 1. Some of the software toolsets were already available in Y1, such as 'mmWaveLink', 'TAISC', though we adapted the names and try to use easy to remember acronyms. Some software components are newly added in Y2, eg the 'LBT', 'SDR-SDN' functionalities are coming from Opencall 1 for Extensions.

The components focusing more on reconfigurability and reprogrammability operation of SDR are highlighted in 'red dashed rectangular'. Please note that the non-highlighted functionalities are not excluded for reconfigurability, however in this work package the focus is on live programming. When clicking on the '+' sign, more details of the specific software components will be displayed, including a short description of the functionality, and the link towards the code repository, the type of the repository, and access condition/permission. The content under 'MySVL' is shown as an example.





+	mmWaveLink
+	GFDM
+	CSMACD
+	CONSENSE
+	IQ switch
+	TAISC
+	Radio-slicing
	M53/I
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Figure 1 ORCA software components, with functionalities for SDR reconfigurability and reprogrammability.

There is one software component that is not made available jet on the ORCA webpage. This is the 'SpecSense' module in RFNoC, developed partially for the DARPA spectrum collaboration challenge. The SpecSense computation engine gives a time average of spectral energy observed. As shown in Figure 2, this module computes FFT magnitude square of the received samples, and averages a certain number (average size) of these blocks before sending them to the host. This not only offloads FFT computation task to the FPGA, but the averaging part also reduces USRP to host data rate. A timestamp is also provided with each SpecSense output packet, which is the timestamp from the first block of received samples used to compute averaged values in that particular packet.







Figure 2 RFNoC SpecSense computation engine

