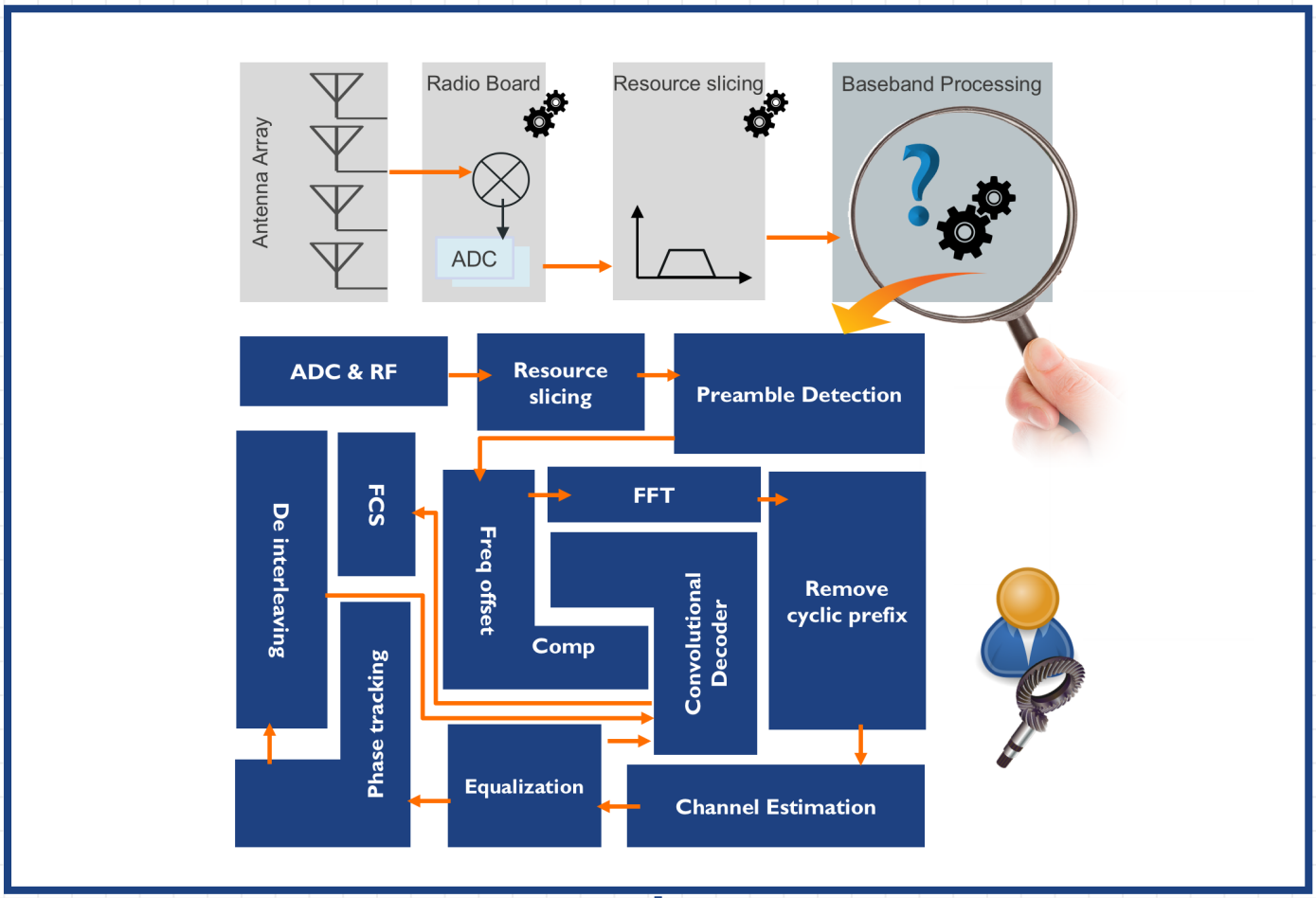
Orchestration and Reconfiguration Control Architecture

SDR DATA PLANE FUNCTIONALITY

Design-time composition: Design-time composition of PHY



- Signal processing chains are divided into micro blocks, such as preamble detection, symbol-level processing, bit-level processing blocks and etc.
- Flexible configuration of PHY can be achieved by configuring the micro processing blocks as well as the routing of samples between the blocks.

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CONTEXT

Today commercialized radio devices are predefined, and each vendor has proprietary designs dedicated to certain types of radio technologies, which are hard to be reused for other purposes afterwards. The direct result is the long development cycle of radio devices. Another noticeable outcome is that there is very limited configurability available for users to customize the radio, resulting suboptimal performance in practical usage. The goal of this offer is to shift composition of PHY in the radio from manufacturing phase to the user, allowing customizing PHY for dedicated applications or research purposes.

UNIQUE SELLING POINT

- Signal processing chains are divided into micro blocks, such as preamble detection, symbol-level processing, bit-level processing blocks and etc.
- Common building blocks between heterogeneous RATs, or between multiple instances of the same RAT, are shared to avoid unnecessary redundancy.
- Flexible configuration of PHY can be achieved by configuring the micro processing blocks as well as the routing of samples between the blocks.
- The routing of samples can be controlled by software, two types of interfaces are considered:
  - via software processor, using DMA connection to transfer samples from one block to another;
  - direct data path can be established between cores, such as the solution offered by RFNoC [1].

OPPORTUNITIES

- This offer enables flexible composition of PHY for different application or research purposes.
- This offer provides possibility for fast prototyping of innovative PHY architectures, hence shortens the development cycle.
- This offer enables designer to optimize resource utilization thanks to possibility of sharing processing blocks.

REFERENCES

The framework is implemented on the Xilinx Zynq ZC706 evaluation board with the Analog Device frontend FMCOMMS2 board, the following steps should be followed to get started:

- a quick scheme through the AD reference design is recommend through this link: https://wiki.analog.com/resources/fpga/docs/hdl
- multiple SDR platforms are available in w-ilab.t testbed, where the Zynq and AD FMCOMMS2 based SDR will also be deployed , http://doc.ilabt.iminds.be/ilabt-documentation/wilabfacility.html

1 Braun, M., Pendlum, J., & Ettus, M. (2016, September). RFNoC: RF network-on-chip. In Proceedings of the GNU Radio Conference (Vol. 1, No. 1).