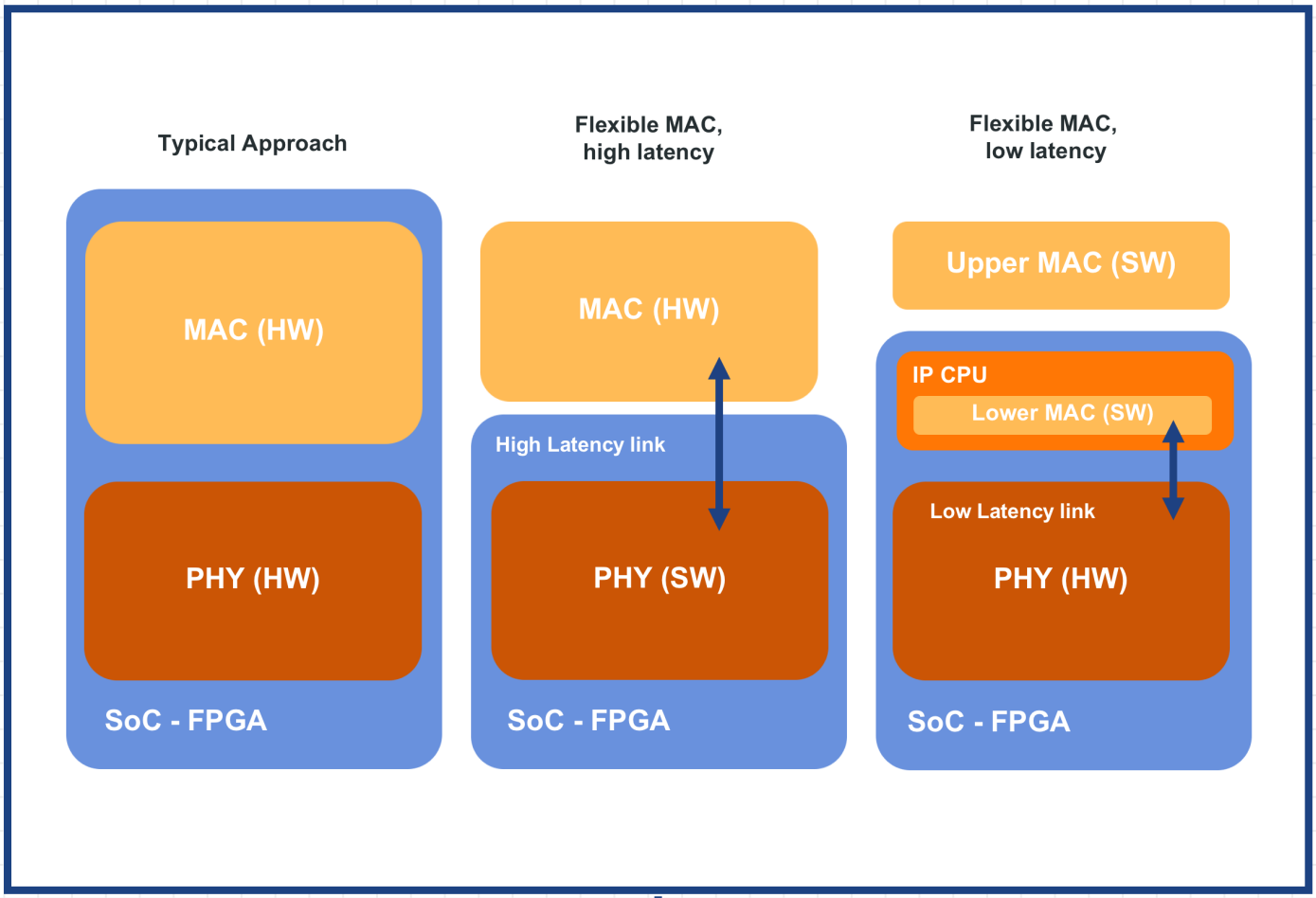
Orca

Orchestration and Reconfiguration Control Architecture

SDR DATA PLANE FUNCTIONALITY

Integration of PHY and upper layer protocols : Low latency PHY and MAC integration



- SoC integration of MAC ad PHY to achieve low latency minimizes flexibility and chance of MAC upgrades
- Software MAC implementations suffer from high communication latency with PHY
- Proposed approach provides low latency with full support of configurability and reprogramming of MAC

SDR DATA PLANE FUNCTIONALITY

Integration of PHY and upper layer protocols: Low latency PHY and MAC integration

CONTEXT

In order to fully exploit a physical medium and to decrease the latency of the employed logic, the lower level MAC core should run as close as possible to PHY. The communication bus between a MAC and the accompanying PHY should be as fast as possible in order to minimize the latency of MAC commands execution. Even more, PHY should be able to provide radio abstractions events and procedures to MAC so that the execution latency of those procedures is also minimal. An example would be “Incoming Frame Detected” and “Clear Channel Assessment”, which are essential for CSMA/CA based technologies [1]. For MAC to be aware of incoming packets the moment they start getting received, PHY should provide such an abstraction and deliver it to MAC in a simple way with minimum latency. On the other hand if “Clear Channel Assessment” procedure is executed on MAC based on a software implementation, the response latency would be high. Thus PHY assisted implementation of such highly PHY dependent procedures should be supported and only the commence of operation and the result should be communicated between PHY and MAC using a simple abstraction primitive. Even more, combining a radio abstraction like “Incoming Frame Detected” and having direct and minimum latency access to the symbols being decoded while the frame is still being received makes it possible to make early decisions based on the frame header content while the frame payload in still in the air and being decoded.
Instead of deploying a specific MAC for every PHY we propose to deploy the lower MAC, namely the TAISC core, on top of every PHY. The TAISC core is a middle layer located at the very lower end of the MAC layer and implements a set of lower MAC primitives that needs to be executed in a certain order. A lower MAC protocol, like CSMA or TDMA, can be defined as a list of these MAC primitives. TAISC can prioritize, switch between MAC protocols and further supports protocol updates. The TAISC core provides generic data and control plane interfaces. Intercommunication between different TAISC cores is generic and straight forward to implement.

UNIQUE SELLING POINT

- Reuse of existing MAC protocols that already have been implemented based on TAISC is possible. The implemented protocols are radio platform independent.
- The TAISC core was designed to run on platforms with constrained resources (msp430 and ARM® Cortex™-M3) but is also available for Xilinx Zynq and runs on one of its ARM® Cortex™-A9 cores. Migration to any other CPU IP core like MicroBlaze should be straightforward.
- To support a new PHY implementation, the Radio module residing in the TAISC core (PHY specific library of MAC primitives) is the only module that will need to be re-implemented in order to take full advantage of the TAISC functionalities.
- The low latency communication provided between MAC and PHY can support high timing requirements from future radios and enable extreme low latency response MAC implementations.

OPPORTUNITIES

By employing such a low latency solution for MAC-PHY communication it will be possible to:

- R&D of MAC protocol to exploit the In Band Full-Duplex technology.
- Experiment with future radios that may require extreme low latency MAC response.

REFERENCES

The framework is implemented on the Xilinx Zynq ZC706 evaluation board with the Analog Device frontend FMCOMMS2 board, the following steps should be followed to get started:

- a quick scheme through the AD reference design is recommend through this link: https://wiki.analog.com/resources/fpga/docs/hdl
- multiple SDR platforms are available in w-ilab.t testbed, where the Zynq and AD FMCOMMS2 based SDR will also be deployed , http://doc.ilabt.iminds.be/ilabt-documentation/wilabfacility.html

1 Crow, B. P., Widjaja, I., Kim, J. G., & Sakai, P. T. (1997). IEEE 802.11 wireless local area networks. IEEE Communications magazine, 35(9), 116-126.