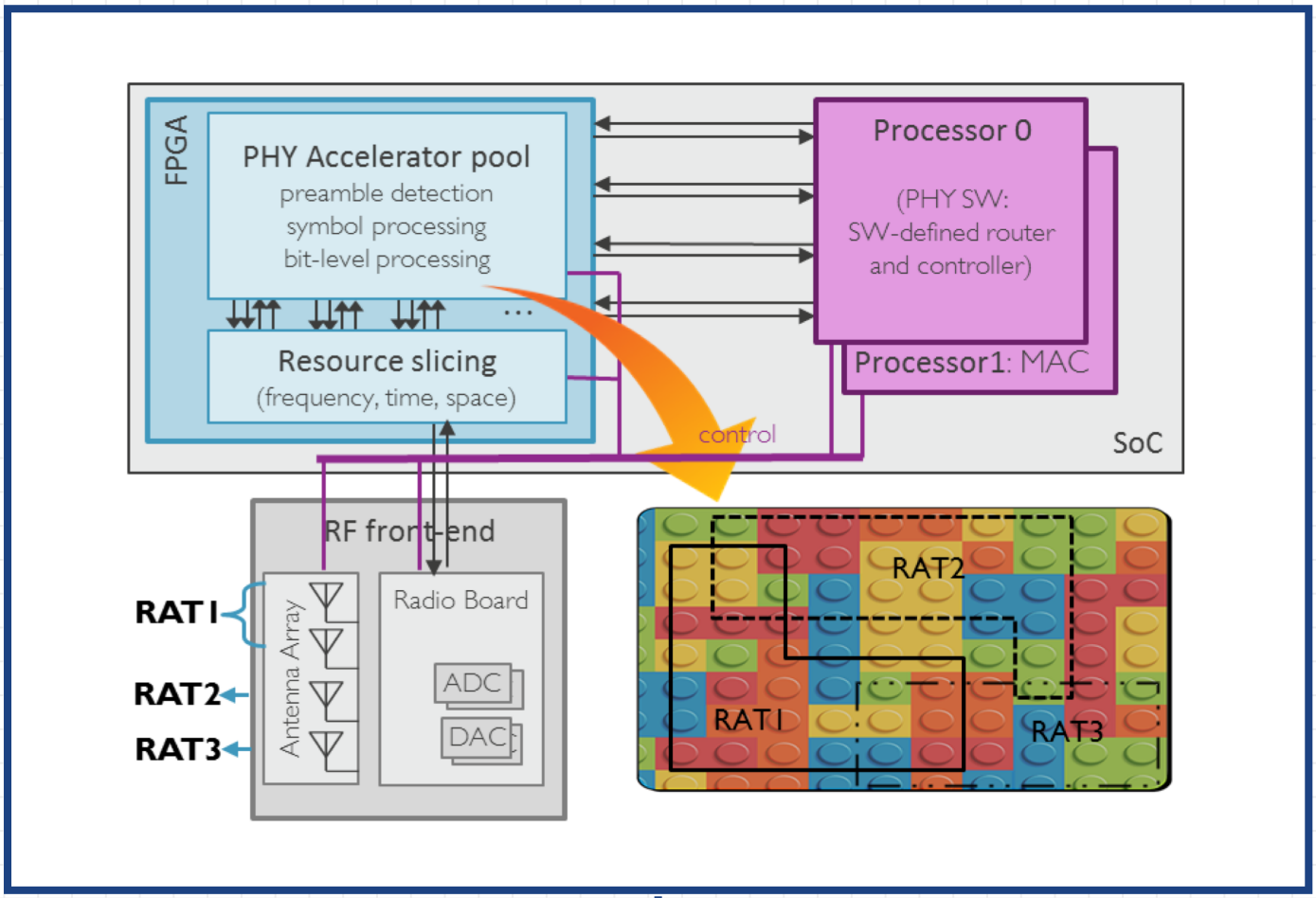
Orca

Orchestration and Reconfiguration Control Architecture

BASIC SDR CONTROL PLANE FUNCTIONALITY

Radio slicing: resource allocation and instantiation

Network slicing



- High level application requirements are for the first time used to drive the hardware utilization and architecture.
- Advanced reconfiguration scheme can be designed by combining the capability of aligning physical and hardware resources with high level end-to-end communication requirements.

BASIC SDR CONTROL PLANE FUNCTIONALITY

Radio slicing: resource allocation and instantiation Network slicing

CONTEXT

Comparing to physical resources, the slicing of radio access network is a relatively new concept. This is because current commercial radio design is implemented as fixed AISC design, there is no possibility of using the same piece of hardware for another purpose. However, for SDR radio design, users do have the flexibility to build the radio architecture from scratch, which leads to the possibility to instantiate single or multiple types of desired RAT (or sub processing modules) according to application requirements. Essentially, the network slicing refers to the slice of complete logical network, including Radio Access Network (RAN) and Core Network (CN). In ORCA, we focus the slicing of RAN, namely the slicing of necessary resources, including SDR hardware resources, processing and memory resources at various levels to serve different traffic flows in RAN. In this offer we aim to present the functionality of network slicing on the ORCA SDR framework.

UNIQUE SELLING POINT

- High level application requirements are for the first time used to drive the hardware utilization and architecture.
- The flexibilities at all network stacks (PHY, MAC, and above layer protocols) of SDR implementation.

OPPORTUNITIES

- Optimizing the usage of limited hardware resources.
- Advanced slice coordination scheme can be built upon flexible network stack.
- Advanced reconfiguration scheme can be designed by combining the capability of aligning physical and hardware resources with high level end-to-end communication requirements.

REFERENCES

The framework is implemented on the Xilinx Zynq ZC706 evaluation board with the Analog Device frontend FMCOMMS2 board, the following steps should be followed to get started:

- a quick scheme through the AD reference design is recommend through this link: https://wiki.analog.com/resources/fpga/docs/hdl
- multiple SDR platforms are available in w-ilab.t testbed, where the Zynq and AD FMCOMMS2 based SDR will also be deployed, http://doc.ilabt.iminds.be/ilabt-documentation/wilabfacility.html