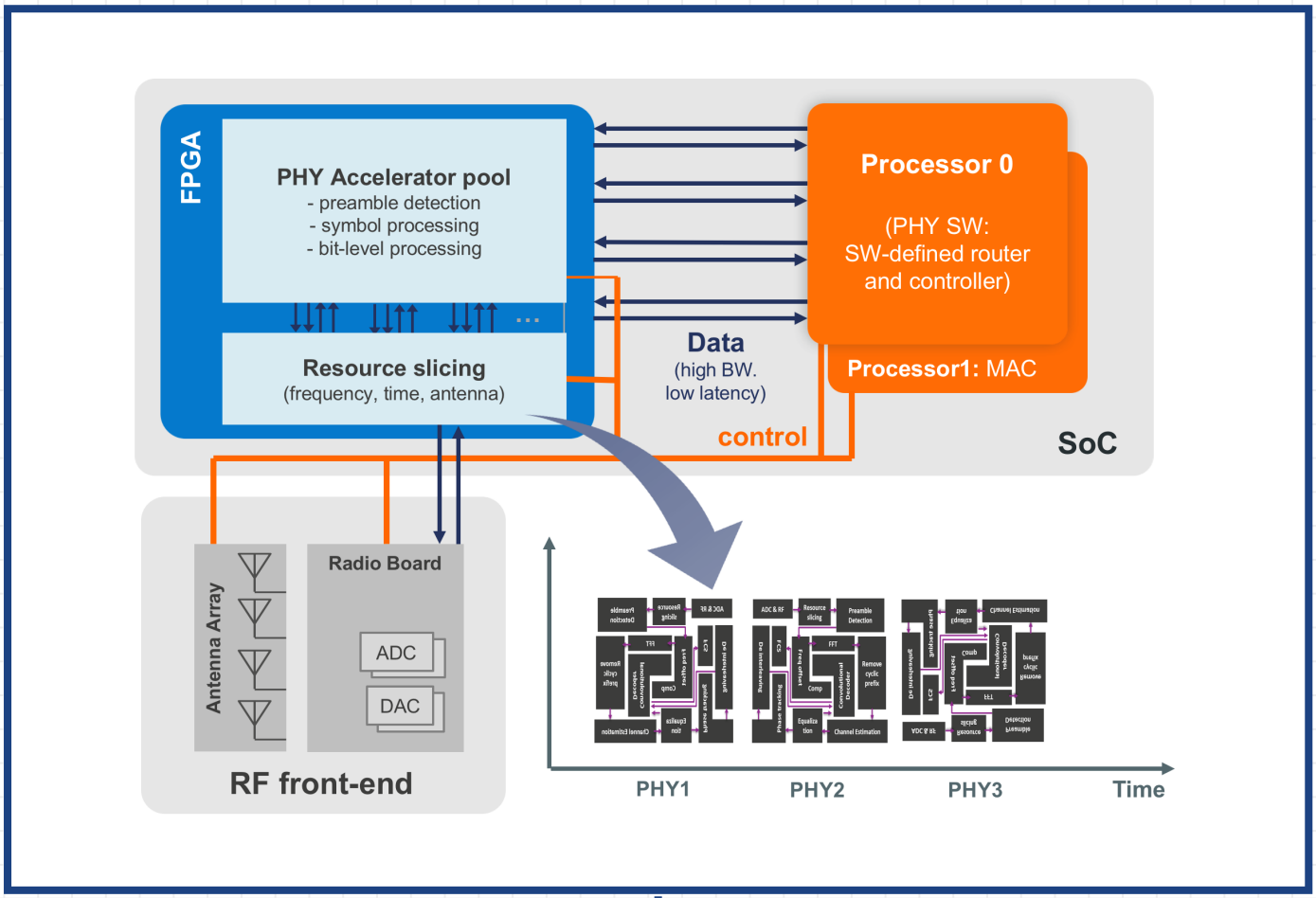
Orca

Orchestration and Reconfiguration Control Architecture

ADVANCED SDR CONTROL AND MANAGEMENT FUNCTIONALITY

Advanced reconfiguration and modular design:
Runtime reconfiguration of PHY transceiver chain



→ Two levels of control can be realized by the software in the ARM core:

- - - - - - → The properties of a particular accelerator, eg FIR filter coefficients or filter depth.

- - - - - - → The routing of data between hardware accelerators.

→ Reconfiguration is realized without changing firmware or FPGA bitstream.

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CONTEXT

In offer 2.3.2 design time composition of PHY, we addressed the need for design time composition of PHY transceiver chain, this offer builds further in this direction. Every static configuration has its limitations, in dynamic environment of wireless communication, there is a need to configure the PHY transceiver chain at run time. This offer presents a PHY transceiver architecture, where PHY processing blocks are executed in hardware, but run-time configuration of processing blocks and routing between blocks is controlled in software.

UNIQUE SELLING POINT

As previously discussed, a transceiver can be composed by many processing blocks, in general three categories are defined, namely the preamble detection, symbol-level and bit-level processing blocks. When these blocks are realized in hardware, more particularly here we used FPGA, they are referred to as hardware accelerators. A collection of various configurable hardware accelerators forms the PHY accelerator pool.
Two levels of configuration can be realized by the software:

- The properties of a particular accelerator, eg FIR filter coefficients or filter depth.
- The routing of data between hardware accelerators, namely recompositing of data path.

Reconfiguration (including recompositing in some implementation) of PHY can be either triggered by pre-defined condition, or triggered by specific commands from the host. In either case, the reconfiguration is realized without changing firmware or FPGA bitstream.

OPPORTUNITIES

- When properly combined with estimation and intelligence modules, this offer allows real time adjustment of PHY according to physical environment, application traffic types, among other influential factors.
- This offer allows real time switching between heterogeneous RATs.

REFERENCES

The framework is implemented on the Xilinx Zynq ZC706 evaluation board with the Analog Device frontend FMCOMMS2 board, the following steps should be followed to get started:

- a quick scheme through the AD reference design is recommend through this link: https://wiki.analog.com/resources/fpga/docs/hdl
- multiple SDR platforms are available in w-ilab.t testbed, where the Zynq and AD FMCOMMS2 based SDR will also be deployed, http://doc.ilabt.iminds.be/ilabt-documentation/wilabfacility.html