

ORCA-PROJECT.EL

LOW LATENCY INDUSTRIAL COMMUNICATION

Seyed Ali Hassani

KU Leuven

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ORCHESTRATION AND RECONFIGURATION CONTROL ARCHITECTURE



- Motivation
- ORCA targets
- What ORCA offers
- Low-latency networking showcase
- A case study with ORCA facilities



Industrial Low Latency Communication



Motivation:

- Collaborative robots in industry
- Cloud-based applications
- Bandwidth intensive applications



Low-latency and reliable communication





Motivation:





ORCA Targets

- Reconfigurable SDRs
- Low latency end-to-end networking
- SDR for short Round Trip Time





What ORCA offers

- Open MAC/PHY for ORCA experimenters
- Modular and Cross-layer MAC-PHY architecture
 - Scalability
 - Easy development
- MAC as close to PHY as possible
 - Low latency
- Run-time programmable MAC
 - Flexibility



ORCA Showcase Overview





ORCA Showcase Overview

Balancing needs low-latency link





ORCA Showcase; MAC and PHY

Flexible GFDM

- PHY and low-level MAC on FPGA
- High-level MAC on host computer
- RTT 1.5 ms





ORCA Showcase; MAC and PHY

Low Cost Flexible and Integrated MAC and PHY

- 802.15.4 PHY on FPGA
- MAC on TAISC processor



ORCA Showcase; MAC and PHY

Cross-layer PHY/MAC Architecture

- 802.15.4 PHY on FPGA
- MAC on Micro blaze softcore
- RTT 1 1.51 ms





ORCA facilities for system level experimentation

KUL testbed







- Pipeline processing
- Heavy data-flow
- Complex control
- Multi-stage procedures
- Interrupt handling
- Flexibility









- High level MAC
 - Backoff time handler
 - Determining Source/Destination
- Low-Level MAC
 - Generating and parsing PHY packet
 - Generating and parsing frame check sequence
 - Interframe time watch





USRP5 USRP3 USRP3 USRP4 USRP5 USRP5

- 4. The SDR sends the balancing commands to the robot
- 3. The process unit generates balancing commands
- Sensor update interval 7 ms
- Unslotted CSMA to share the channel (2.4 GHz)
- Imm-Ack packet to transmit balancing commands



	MicroBlaze	+ MicroBlaze
	One layer MAC	Tow-layer MAC
Time to generate ACK packet and pass it to the packet queue	10-16 µs	0.41 µs
FPGA Resource consumption	8%	< (8+2)%
Packet loss rate (4 nodes)	3.5%	< 0.4%

- Reliability + latency improvement
- Scalable low-level MAC
 - Multi-channel & full-duplex MAC schemes



Demo in CROWNCOM

Low latency communication over a single band;

- Two robots and 4 radio links
- Contention-based network ; unslotted CSMA/CA





Thank you for your attentions!



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Questions!?